A Review of FPGA-Oriented Network-on-Chip Routing Algorithms & Topographies

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Motivation

- Advances in semiconductor manufacturing, demand for novel acceleration hardware (i.e. AI), and computer architecture are driving up core count.

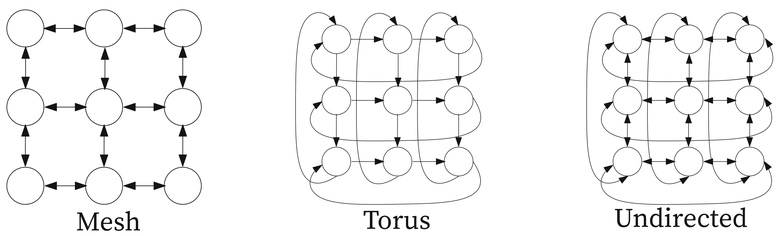
- Existing core-to-core interconnects do not scale adequately to very high core-count architectures.

- NoCs (Network on Chip) attempt to alleviate this by replacing crossbar-switch based approaches with routed network fabrics.

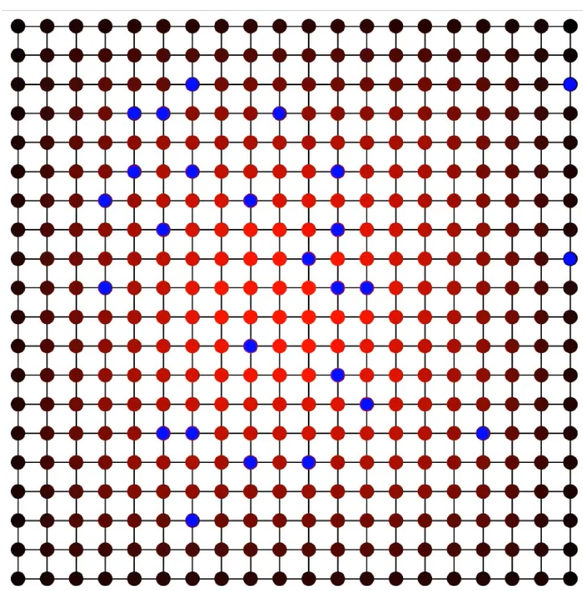
- Most NoC implementations still use significant amounts of hardware resources, reducing those available for acceleration cores.

- Bufferless NoCs reduce usage of hardware resources by eliminating storage requirements for routing buffers, and instead intentionally misrouting flits when an optimal outgoing link is unavailable.

NoC Topographies



Contention Heatmap



Problem

- We wish to establish a clear correlation between different routing strategies and network topographies in bufferless NoCs and NoC performance.

Approach

- We have implemented a custom software simulator (nocsim) which allows the simulation of (nearly) arbitrary NoC topographies and routing behaviors.

- To demonstrate the soundness of nocsim as a foundation for future work, we reproduce the results obtained via the state-of-the-art Hoplite NoC implementation[1].

nocsim

- nocsim is implemented in the C programming language, and is open source. It may be downloaded from https://github.com/herclab/nocsim

- nocsim guarantees deterministic simulation results, and generates output in a simple, easy-to-process format.

- While this work examines only a handful of common routing strategies and network topographies, nocsim is capable of accurately simulating nearly any two-dimensional network topogrophy, and can easily be extended to support additional routing behaviors.

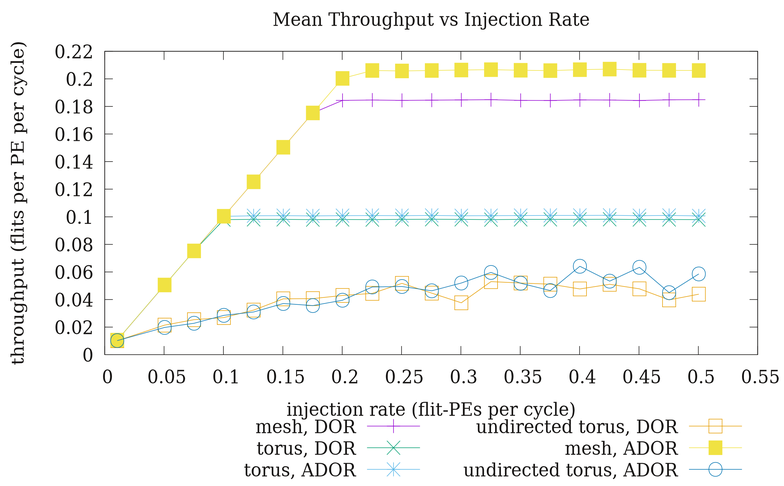
Results

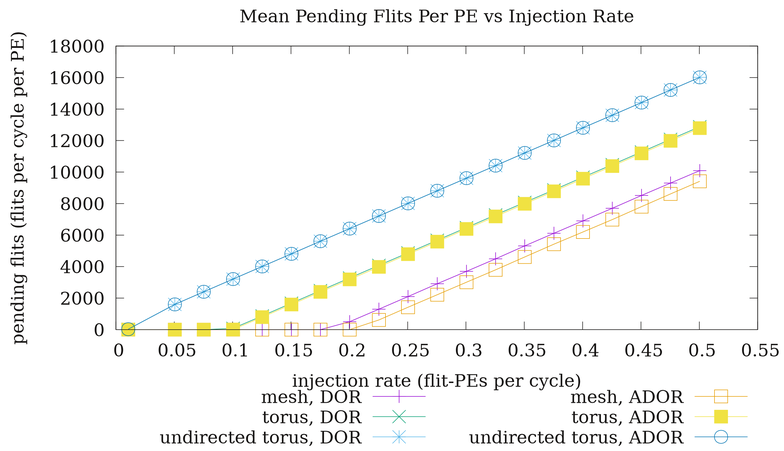
- We successfully re-produced the results described in [1] with the Hoplite NoC for the directed torus configuration with DOR routing.

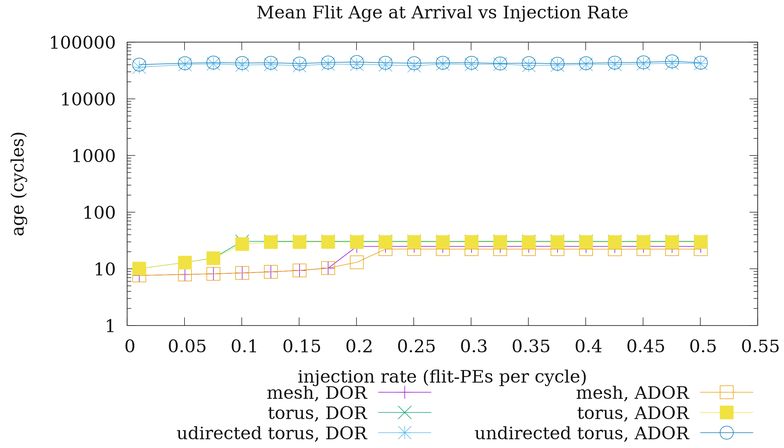
- Results demonstrate a clear correlation between injection rate and the inflection point after which network performance breaks down.

- Results relating to the underacted torus topography are anomalous, and require further research and investigation

Results







References

[1] N. Kapre and J. Gray, “Hoplite: A Deflection-Routed Directional Torus NoC for FPGAs,” ACM Transactions on Reconfigurable Technology and Systems, vol. 10, no. 2, pp. 1–24, Mar. 2017.

[2] J. Lin, X. Lin, and L. Tang, “Making-a-stop: A new bufferless routing algorithm for on-chip network,” Journal of Parallel and Distributed Computing, vol. 72, no. 4, pp. 515–524, Apr. 2012.